PRINCIPLES OF CMOS VLSI DESIGN

A Systems Perspective

Second Edition

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diffused regions. The gate is a control input—it affects the flow of electrical current between the source and the drain. In fact, the drain and source may be viewed as two switched terminals. They are physically equivalent; the name assignment depends on the direction of current flow. For now, we will regard them as interchangeable. The fourth terminal of an MOS transistor, the substrate will be ignored for this discussion.

1.4 MOS Transistor Switches

The gate controls the passage of current between the source and the drain. Simplifying this to the extreme allows the MOS transistors to be viewed as simple on/off switches. In the following discussion, we will assume that a '1' is a high voltage that is normally set to a value between 1.5 and 15 volts and called POWER (PWR) or V_{DD}. The symbol '0' will be assumed to be a low voltage that is normally set to zero volts and called GROUND (GND) or V_{SS}. The strength of the '1' and '0' signals can vary. The "strength" of a signal is measured by its ability to sink or source current. In general, the stronger a signal, the more current it can source or sink. By convention, current is sourced from POWER and GROUND sinks current. Where the terms *output* and *input* are used, an output will be a source of stronger '1's and '0's than an input. The power supplies (V_{DD} and V_{SS}) are the source of the strongest '1's and '0's.

The nMOS switch (N-SWITCH) is shown in Fig. 1.2(a). The conventional schematic icon representation is shown along with that for the switch notation. The gate has been labeled with the signal s, the drain a, and the source b. In an N-SWITCH, the switch is closed or 'ON' if the drain and the

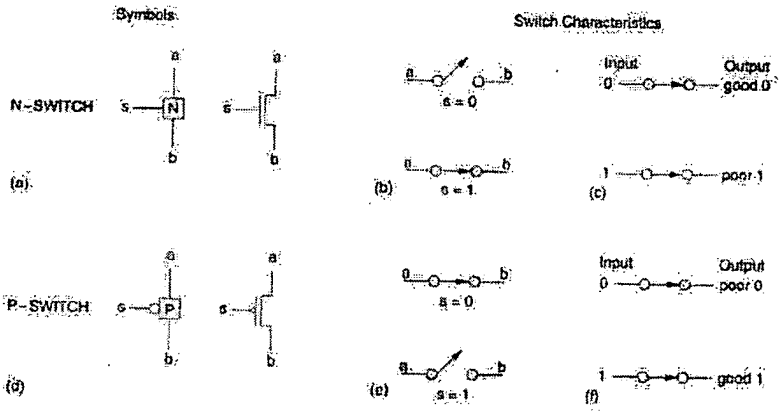

FIGURE 1.2 nMOS and pMOS switch symbols and characteristics

source are connected. This occurs when there is a '1' on the gate. The switch is open or 'OFF' if the drain and source are disconnected. A '0' on the gate ensures this condition. These conditions are summarized in Fig. 1.2(b). An N-SWITCH is almost a perfect switch when a '0' is to be passed from an output to an input (say a to b in Fig. 1.2b). However the N-SWITCH is an imperfect switch when passing a '1.' In doing this, the '1' voltage level is reduced a little (this is explained in Section 2.5). These cases are shown in Fig. 1.2(c). The pMOS switch (P-SWITCH) is shown in Fig. 1.2(d). It has different properties from the N-SWITCH. The P-SWITCH is closed or 'ON' when there is a '0' on the gate. The switch is open or 'OFF' when there is a '1' on the gate. Figure 1.2(e) depicts these conditions. Notice that the pMOS and nMOS switches are ON and OFF for complementary values of the gate signal. We denote this difference for a P-SWITCH by including the inversion bubble in the schematic icon notation. A P-SWITCH is almost perfect for passing '1' signals but imperfect when passing '0' signals. This is illustrated in Fig 1.2(f).

The output logic levels of an N-SWITCH or a P-SWITCH are summarized in Table 1.1.

By combining an N-SWITCH and a P-SWITCH in parallel (Fig. 1.3a), we obtain a switch in which '0's and '1's are passed in an acceptable fashion (Fig. 1.3b). We term this a complementary switch, or C-SWITCH. In a circuit where only a '0' or a '1' has to be passed, the appropriate subswitch (n or p) may be deleted, reverting to a P-SWITCH or an N-SWITCH. Note that a double-rail logic is implied for the complementary switch (the control input and its complement are routed to all switches where necessary. The control signal is applied to the n-transistor and the complement to the p-transistor). The complementary switch is also called a transmission gate or pass gate (complementary). Commonly used schematic icons for the transmission gate are shown in Fig. 1.3(c).

TABLE 1.1 The Output Logic Levels of N-SWITCHES and P-SWITCHES

LEVEL	SYMBOL	SWITCH CONDITION
Strong 1	1	P-SWITCH gate = 0, source = V_{DD}
Weak 1	1	N-SWITCH gate = 1, source = V_{DD} or P-SWITCH connected to V_{DD}
Strong 0	0	N-SWITCH gate = 1, source = V_{SS}
Weak 0	0	P-SWITCH gate = 0, source = V_{SS} or N-SWITCH connected to V_{SS}
High impedance	Z	N-SWITCH gate = 0 or P-SWITCH gate = 1